

New Resonance Type Fault Current Limiter

Mehrdad Tarafdar Hagh¹, Member, IEEE, Seyed Behzad Naderi² and Mehdi Jafari², Student Member, IEEE

¹Mechatronic Center of Excellence, University of Tabriz, Tabriz, IRAN

²Faculty of Electrical and Computer Engineering, University of Tabriz, Tabriz, IRAN

Emails: tarafdar@tabrizu.ac.ir, s.b.naderi87@ms.tabrizu.ac.ir, m.jafari87@ms.tabrizu.ac.ir

Abstract—This paper proposes a new parallel LC resonance type Fault Current Limiter (FCL). This structure has low cost because of using dry capacitor and non-superconducting inductor and fast operation. The proposed FCL is able to limit fault current in constant value near to pre-fault condition value against series resonance type FCL. In this way, the voltage of point of common coupling (PCC) will not change during fault. Analytical analysis is presented in detail and simulation results are involved to validate the effectiveness of this structure.

Keywords—resonance circuit; fault current limiter; dc reactor; total harmonic distortion

I. INTRODUCTION

Growth of power transmission and distribution systems has resulted in a continuous increase in short circuit currents level [1]. The most common ways to limit high-level fault currents are: upgrading of switchgear and other equipments, splitting the power grid, introducing higher voltage connections (ac or dc), using high-impedance transformers and etc. These alternatives may create other problems such as loss of power system safety, reliability, high cost and more power losses. In such condition, the realization of a FCL is going to be expected, strongly. The SFCL structures offer a good way to limit the fault currents level in distribution networks due to natural low- losses in superconductors during the normal operation [2].

The implementation of FCLs in electric power systems is not restricted to suppress the amplitudes of the short circuits; they are also utilized to variety of performances such as the power system transient stability enhancement, power quality improvement, reliability improvement, increasing transfer capacity of system equipment and inrush current limitation in transformers [3]–[6]. An ideal FCL should have the following characteristics [2]:

- 1) Zero impedance at normal operation;
- 2) No power loss in normal operation;
- 3) Large impedance in fault conditions;
- 4) Quick appearance of impedance when fault occurs;
- 5) Fast recovery after fault removal;

Resonance type superconducting FCLs have been proposed in literatures [7], [8]. These types of FCLs limit fault current by using various topologies of series LC resonant circuits.

In this paper new structure of parallel LC resonance type FCL is proposed. Series resonance type FCL limits fault current and does not allow the short circuit current to increase

instantaneously. It is important to note that, if fault continues, series resonance type FCL will not be able to limit level of fault current, so we propose parallel LC resonance type FCL. Parallel LC circuit offers high impedance at resonant condition. It can limit fault currents by selecting various values for L and C. This type of FCL has high flexibility for fault current limiting purposes. Indeed, by using the proposed FCL, fault current will always have constant value against series resonance type of FCL. Analytical analysis and design considerations are presented and their solution is done by MATLAB software. The circuit operation in normal and fault conditions are simulated by using EMTDC/PSCAD.

II. POWER CIRCUIT TOPOLOGY AND OPERATION PRINCIPLES

Fig. 1 shows single phase power circuit topology of proposed FCL.

This structure is composed of two main parts which are described as follows:

1) Bridge part: This part consists of a Semi-Conductor Rectifier (SCR) bridge containing D_1 to D_4 diodes, a superconducting dc limiting reactor (L_{dc}), an IGBT switch, a dc voltage source and a freewheeling diode (D_f).

2) Resonance part: This part consists of a parallel LC resonant circuit that is tuned on 50 Hz network frequency and a resistor in series with the capacitor.

Bridge part of FCL operates as a high speed switch that changes fault current path to resonant part, when fault occurs. Obviously, as a conventional method, it is possible to substitute this part with an anti parallel connection of two semiconductor switches. In this case, it is necessary to use a series inductor with each switch for limiting severe di/dt .

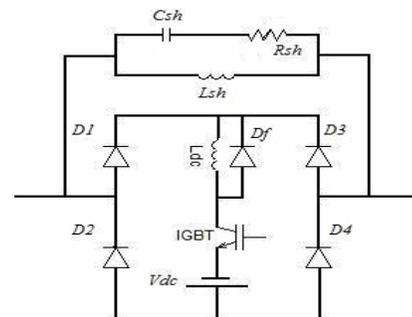


Figure 1. Power circuit topology of new proposed resonance type FCL

These inductors make a voltage drop on FCL and affect FCL's operation in normal state. But, using diode rectifier bridge and placing IGBT in this bridge has two advantages as follows:

1) This structure uses only one controllable semiconductor device which operates at dc side, instead of two switches that operate at ac current. So, control circuit is simpler because of no need to switching ON/OFF at normal operation case. In addition, there is not switching losses.

2) It is possible to placing a small reactor in series with IGBT at dc side. This reactor plays two roles; Snubber for IGBT to protect it and current limiter at first moments of fault that will be discussed in detail.

In this structure, by IGBT as a self turn-off device, operation delay problem of FCL is mitigated.

The dc voltage source is used to compensate the voltage drop on diodes and IGBT. So its value is defined as follow:

$$V_{dc} = 2V_{DF} + V_{SW} \quad (1)$$

Where V_{SW} stands for the voltage drop across IGBT and the forward voltage drop across rectifier diodes is defined as V_{DF} .

Fig. 2 shows that by placing dc voltage source in proposed FCL topology, THD and distortion of load voltage is reduced [2].

This is important to note that dc voltage source can be provided by diode rectifiers [3].

In normal operation of power system, small dc reactor charges to the peak of line current and behaves as short circuit. On the other hand, the dc voltage source compensates the voltage drop on diodes and IGBT switch. So, voltage drop on the bridge becomes almost zero. Consequently FCL does not affect normal operation of system.

As fault occurs, dc reactor limits short circuit current and starts to charge. When the line current rises to the pre-defined value that can be set by system operator, control system turns off the IGBT switch. So, the bridge retreats from the utility. At this moment, freewheeling diode turns on and provides free path for discharging dc reactor.

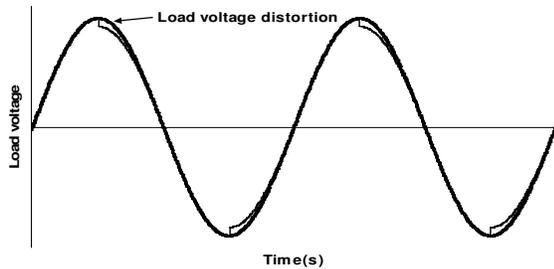


Figure 2. Load voltage with (—) and without (---) dc voltage source

When the bridge turns off, fault current go through the parallel resonant part of FCL. Consequently, large impedance enters to the circuit and prevents rising the fault current.

It is obvious that, in fault condition, parallel LC circuit starts to resonance. In this case, because of resonance, line current oscillates with large amplitude that passes from power system equipments. This may lead to harm them or put them in stress. But, by placing a resistor (R_{sh}) in series with the capacitor, transient swings of current damp quickly.

Some previous structures have ac power losses at resonant circuit in no-fault condition, because of placing large inductor in line current path [9], [10]. But, this structure has very lower losses in normal condition. Also, during fault, proposed FCL behaves in a way that power system is not affected by fault current. So, there will not be any voltage sag on PCC voltage.

In addition, at pervious structures, capacitor is in power system, always. So, oil capacitor must be used. But capacitor of this structure is bypassed at normal operation of power system and dry capacitor with low cost can be used.

III. ANALYTICAL ANALYSIS

Fig. 3 shows the single phase power system model of proposed FCL. The utility voltage is a three-phase sinusoidal waveform where ω and V_s stand for its angular frequency and effective voltage value in each phase, respectively. The utility impedance is modeled by series connection of a resistor R_s and an inductor L_s .

Analytical analysis is discussed in three modes as follows:

Mode 1: Pre-fault steady state operation.

Mode 2: Just after fault occurrence until IGBT turning off.

Mode 3: Between IGBT turning off and fault removal.

A. Mode 1

In normal operation of power system, as discussed, SCR bridge bypasses resonant circuit. In this condition, line current (i_L) can be expressed by differential equation (2):

$$V_s \sin(\omega t) = Ri_L + \omega L (di_L / d\omega t) \quad (2)$$

where:

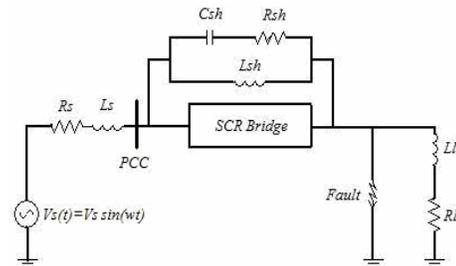


Figure 3. Single phase power system model

$R = R_s + R_L$ (Resistance of source and load, respectively)

$L = L_s + L_L$ (Inductance of source and load, respectively)

V_s : RMS of utility voltage

So the line current equation can be derived as:

$$i_L(\omega t) = (V_s / \sqrt{R^2 + \omega^2 L^2}) [(L\omega / \sqrt{R^2 + \omega^2 L^2}) e^{-(R/\omega L)\omega t} + \sin(\omega t - \varphi)] \quad (3)$$

where:

$$\varphi = \arctan(\omega L / R) \quad (4)$$

B. Mode 2

When a short circuit occurs, the dc limiting reactor can limit the increasing rate of fault current. The IGBT switch doesn't operate until line current reach to per-defined value. Since time interval of fault occurrence instant to IGBT operation is very small, its analysis is not presented in detail in this paper.

C. Mode 3

After IGBT operation, the bridge is switched off and the dc limiting reactor retreats from the utility; then, the fault current is limited by the resonant circuit. So, differential equation of fault current can be expressed as follow:

$$\begin{cases} L_s L_{sh} C_{sh} (d^3 i_L / dt^3) \\ + (R_s L_{sh} C_{sh} + L_s R_{sh} C_{sh} + R_{sh} L_{sh} C_{sh}) (d^2 i_L / dt^2) \\ + (L_s + R_{sh} C_{sh} R_s + L_{sh}) (di_L / dt) + R_s i_L = \\ (V_s - L_{sh} C_{sh} \omega^2) \sin(\omega t) + R_{sh} C_{sh} V_s \omega \cos(\omega t) \end{cases} \quad (5)$$

With initial values as follows:

$$\begin{cases} i_L(t = t_{sw}) = I_0 \\ (di_L / dt)(t = t_{sw}) = (V_s \sin(\omega t_{sw}) - I_0 (R_s + R_{sh})) / L_s \\ (d^2 i_L / dt^2)(t = t_{sw}) = (V_s \omega \cos(\omega t_{sw}) \\ + I_0 ((R_{sh}^2 / L_{sh}) - (1 / C_{sh})) \\ - ((V_s \sin(\omega t_{sw}) - I_0 (R_s + R_{sh})) / L_s) (R_{sh} + R_s) \end{cases} \quad (6)$$

Where:

I_0 : Pre-defined line current;

t_{sw} : IGBT switch turn off instant.

Equation (5) is solved by MATLAB software and its results are presented in simulations section. In addition, the calculation results of MATLAB and simulations of PSCAD are compared together to prove accuracy of analytical analysis. As mentioned before, using resistor in proposed resonant structure, can damps transient swings in primal cycle of fault. After removal of this transient state, the equation of fault current can be expressed by:

$$i_L = A \cos(\omega t) + B \sin(\omega t) \quad (7)$$

where:

$$\begin{aligned} A &= \frac{V_s [R_{sh} C_{sh} \omega (d' - b' \omega^2) - (1 - L_{sh} C_{sh} \omega^2) (c' \omega - a' \omega^3)]}{(c' \omega - a' \omega^3)^2 + (d' - b' \omega^2)^2} \\ B &= \frac{V_s [R_{sh} C_{sh} \omega (a' \omega^3 - c' \omega) - (1 - L_{sh} C_{sh} \omega^2) (d' - b' \omega^2)]}{(c' \omega - a' \omega^3)^2 + (d' - b' \omega^2)^2} \\ a' &= L_s L_{sh} C_{sh}, \\ b' &= R_s L_{sh} C_{sh} + L_s R_{sh} C_{sh} + R_{sh} L_{sh} C_{sh}, \\ c' &= L_s + R_{sh} C_{sh} R_s + L_{sh}, \\ d' &= R_s \end{aligned} \quad (8)$$

Considering (7) and choosing proper values for L_{sh} and C_{sh} , it is possible to limit the line current in fault condition in a way that its value be near to the pre-fault line current. In this state, if fault occurs, PCC voltage will not sense the fault.

IV. SIMULATION RESULTS AND DESIGN CONSIDERATIONS

The power circuit topology of Fig. 3 is used for simulation in fault condition. The simulation parameters are as follows:

System parameters:

$$V_s = 6.6kV (rms), Z_{source} = 0.57 + j\omega 0.003\Omega$$

$$Z_{load} = 15 + j\omega 0.1\Omega$$

$$Z_{Fault} = 0.01 + j\omega 0.001\Omega$$

$$Z_{line} = 0.5\Omega$$

FCL parameters:

$$R_{sh} = 16\Omega, C_{sh} = 150\mu F, L_{sh} = 68mH$$

$$L_{dc} = 10mH$$

$$V_{DF} = V_{SW} = 3V$$

$$I_0 = 500A$$

Fault occurs at 1.005s and lasts 0.12s (6 cycles of power frequency).

As fault occurs, without using FCL, fault current increases extremely (Fig. 4a). Also, without using R_{sh} in resonance circuit, transient oscillations appear on the line current caused

by LC resonance as shown in Fig. 4b. After damping of these transients, line current becomes a small value.

Fig. 4c shows the line current in fault condition with using proposed resonant type FCL. As shown in Fig. 4c, when fault current reaches to I_0 that is the pre-defined fault level, IGBT turns off (at $t_{sw} = 1.0052s$) and line current is mitigated in fault condition. After fault removal, IGBT turns on again and line current returns to the normal state, after negligible distortion.

Fig. 5 shows dc reactor current. As fault occurs, it starts to charge until IGBT turning off. Then freewheeling diode turns on and discharges dc reactor. After fault removal, dc reactor recharges because of resonant circuit voltage. With discharging resonant circuit, dc reactor current discharges and returns to normal state. Fig. 6 shows PCC voltage with and without proposed structure. As shown in this figure, proposed FCL can prevent voltage sag on PCC, properly.

To demonstrate the accuracy of calculations, differential equation (5) that shows the line current in fault condition, is solved by MATLAB software and result is displayed in Fig. 7.

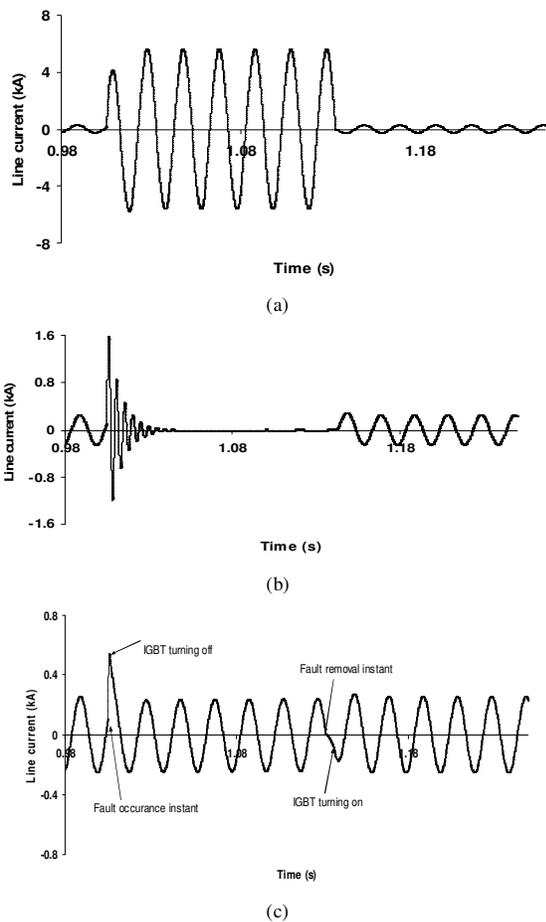


Figure 4. Fault current (a) without FCL (b) without R_{sh} in resonant type FCL (c) with proposed FCL

This figure is in accordance with Fig. 4c. Values and variation of curve shows that result of calculations are adapted by simulation result of PSCAD.

Fig. 8 used to choose proper values for C_{sh} , L_{sh} and R_{sh} . Curves are plotted for R_{sh} from 10 to 100 ohms. Lower limit of R_{sh} is selected to ensure proper transient response of resonant circuit. Standard values for C_{sh} is obtained from [11].

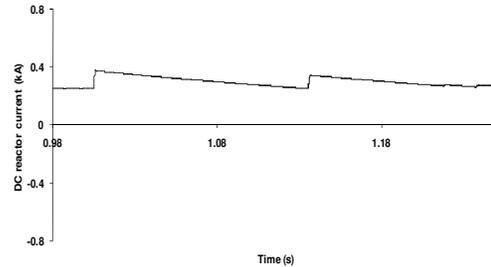


Figure 5. Dc reactor current

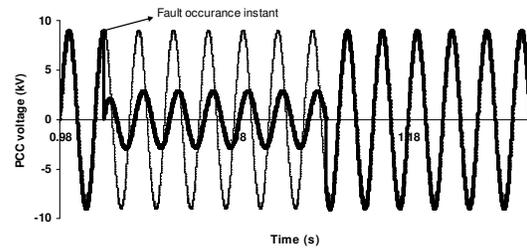


Figure 6. PCC voltage without (—) and with (---) proposed topology

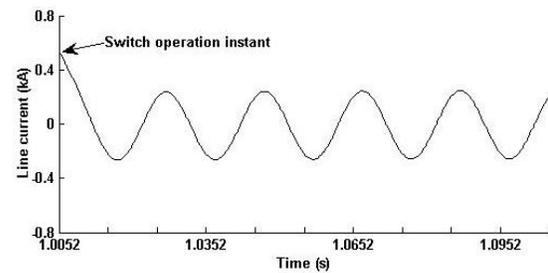


Figure 7. Fault current calculated by MATLAB

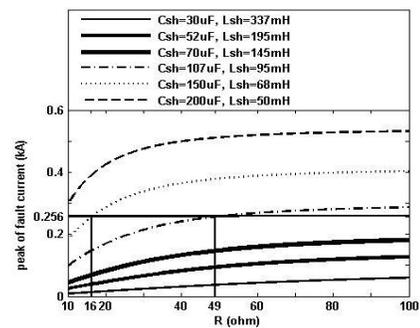


Figure 8. Variation of fault current respect to R_{sh}

It is considered that feeder's average current is 256A at test system. In this condition, pre-desired value of fault current (256A) can be achieved by two values for resonant circuit parameters as follows:

Case 1: $C_{sh} = 150\mu F$, $L_{sh} = 68mH$, $R_{sh} = 16\Omega$

Case 2: $C_{sh} = 107\mu F$, $L_{sh} = 95mH$, $R_{sh} = 49\Omega$

In case (1), R_{sh} is smaller than its value in case (2). So, generated heat in R_{sh} is reduced in fault condition. As a result, design of R_{sh} becomes simpler.

However, we can choose another values for R_{sh} , for example lower than 16Ω , in this case (As shown in Fig. (8)), line current in fault condition will be lower than pre-fault condition value. In addition, transient swings of fault current will be increase.

V. HARMONIC STUDY

As explained previously, using the dc voltage source in proposed structure and compensation of voltage drop on semiconductor devices reduces THD of voltage waveform. Magnitude of dc voltage source obtains from (1).

Fig. 9 shows the frequency spectrum of load voltage in normal operation of power system with and without dc voltage source. As shown in Fig. 2 and Fig. 9, by using dc voltage source in proposed topology, the distortions of voltage waveform in normal operation are decreased to lower values. Simulation results prove this statement as follows:

Load voltage THD, without dc voltage source: 1.98%

Load voltage THD, with dc voltage source: 0.061%

It is important to note that the THD of load voltage is near to zero for proposed structure.

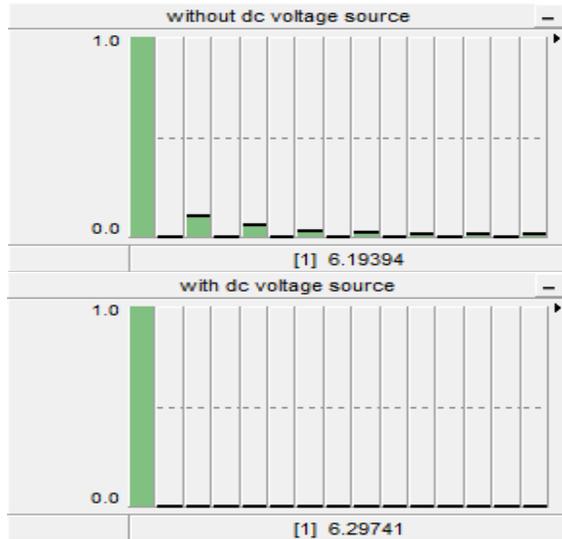


Figure 9. Frequency spectrum of load voltage (kV)

VI. CONCLUSIONS

In this paper, a new topology of parallel LC resonant type fault current limiter that includes a series resistor with the capacitor of LC circuit is introduced. The analytical analysis and design considerations for this structure of FCL are presented. The overall operation of mentioned FCL in normal and fault cases are studied in detail. Proposed resonant type FCL can limit fault current in a way that PCC voltage doesn't change during fault. This means that, in case of transient faults, it is not necessary to open the line. By using R_{sh} in proposed topology, transient swings of current caused by resonance just after fault damps quickly. In addition, this structure has low losses, low harmonic distortion, low cost because of using dry capacitor and non-superconducting inductor, fast operation because of using IGBT switch and capable of controlling fault current at constant value against series resonant type FCLs. In general, proposed resonant type FCL has high flexibility for fault current limiting aims.

REFERENCES

- [1] Zhang Xiaoqing, Ming Li, "Using the Fault Current Limiter With Spark Gap to Reduce Short-Circuit Currents," *IEEE Trans. Power Del.*, vol. 23, no. 1, pp. 506-507, January 2008.
- [2] M. Tarafdar Hagh, M. Abapour, "Non-superconducting fault current limiters," *Euro. Trans. Electr. Power*, Published online in Wiley InterScience, pp. 669-682, March 2008.
- [3] Mehrdad Tarafdar Hagh, Mehdi Abapour, "Nonsuperconducting Fault Current Limiter With Controlling the Magnitudes of Fault Currents," *IEEE Trans. Power Elec.*, vol. 24, no. 3, pp. 613-619, March 2009.
- [4] M. M. R. Ahmed, G. A. putrus, L. Ran, "Power Quality Improvement Using Solid State Fault Current limiter," *IEEE, Transmission and Distribution Conference, Asia Pacific*, vol. 2, pp. 1059-1064, Oct. 2002.
- [5] M. Tarafdar Hagh and M. Abapour, "DC reactor type transformer inrush current limiter," *IET Electr. Power*, vol. 1, no. 5, pp. 808-814, Appl., 2007.
- [6] M. Tsuda, Y. Wilitani, K. Tsuji, K. Kakihana, "Application of Resistor Based Superconducting Fault Current Limiter to Enhancement of Power System Transient Stability," *IEEE Trans. Appl. Supercond.*, vol. 11, no. 1, pp. 2122-2125, March 2001.
- [7] K. Arai, H. Tanaka, M. Inaba, "Test of Resonance-Type Superconducting Fault Current Limiter," *IEEE Trans. Appl. Supercond.*, vol. 16, no. 2, pp. 650-654, June 2006.
- [8] H. Arai, M. Inaba, T. Ishigohka, "Fundamental Characteristics of Superconducting Fault Current Limiter Using LC Resonance Circuit," *IEEE Trans. Appl. Supercond.*, vol. 16, no. 2, pp. 642-646, June 2006.
- [9] Hector G. Sarmiento, "A Fault Current Limiter Based on an LC Resonant Circuit: Design, Scale Model and Prototype Field Tests," *iREP Symposium-Bulk Power System Dynamics and Control-VII, Revitalizing Operational Reliability*, pp. 1-5, August 2007.
- [10] S. Henry, T. Baldwin, "Improvement Of Power Quality By Means Of Fault Current Limitation," *IEEE, System theory, Proceedings of the Thirty-Sixth Southeastern Symposium on*, pp. 280-284 2004.
- [11] High Voltage Capacitors and Power Supplies, *General Atomics, Electronics Systems*, gaep.com